**Digital Logic Design Lab # 12**

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***Lab Section: B***

***LabTitle:***

1. Verify the operation of Multiplexer
2. Construct an 8-to-1 multiplexer using two 4-to-1 multiplexers and implement a four-input Boolean function on it.

***Objectives:***

* Practicing the implementation of logic functions using MSI level functional blocks  Gaining a close insight into the functioning and properties of multiplexer (MUX) circuits  Developing skills in the design and testing of combinational logic circuits.

***Equipment Required:***

* DEV-2765E Trainer Board
* 74LS04 Hex Inverter
* 74LS153 (dual 4-to-1 Multiplexer)

***Background Theory***

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs the information to a single output line. The selection of a particular input line is controlled by a set of input variables, called selection input. Normally, there are 2n input lines and n selection inputs whose bit combination determines which input is selected.

A demultiplexer is doing the opposite function of multiplexer. It takes input on a single input line and the select lines determines one of the 2n output lines and the input contents is visible on that particular output.

Construct an 8-to-1 multiplexer using two 4-to-1 multiplexers, and then implement the following four- input function with a multiplexer.

*F (A, B, C, D) = ∑m (2, 3, 5, 6, 8, 9, 12, 14)*

**Pin Configuration of 74153 (4-to-1 Multiplexer)**

S

0

S

1

D

0

D

1

D

2

D

3

Y

Vcc

GND

E

1

14

2

6

5

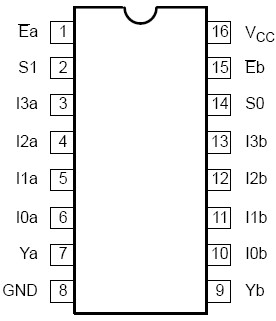
4

3

8

16

7



74153

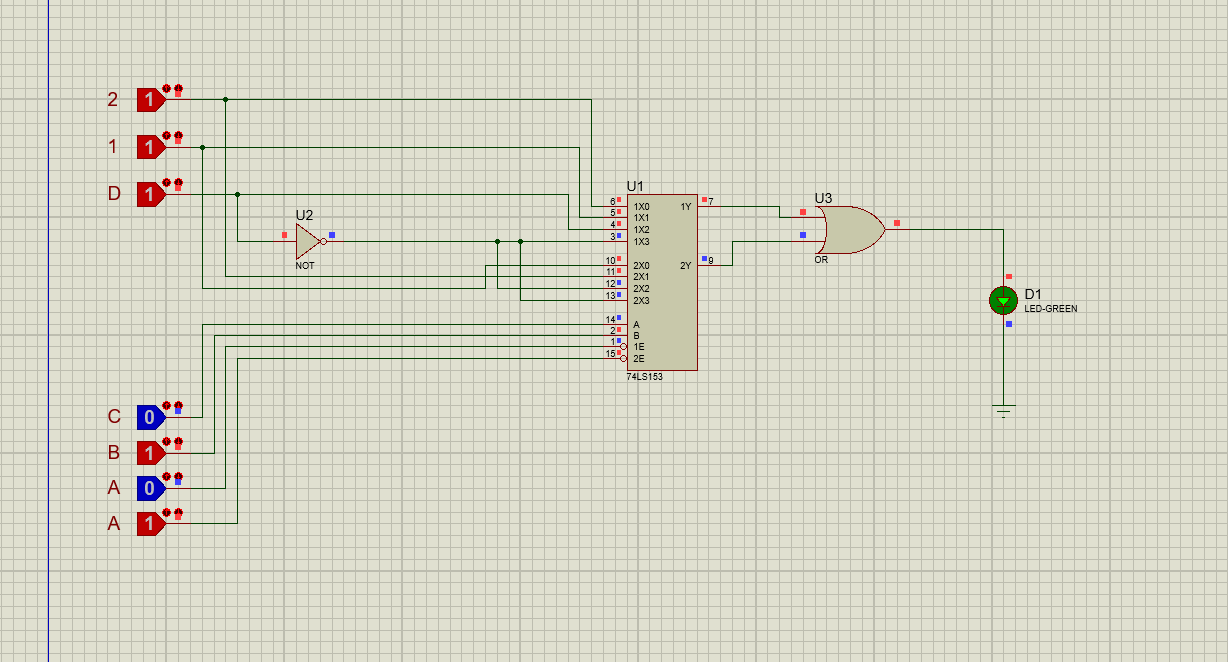
|  |  |  |  |
| --- | --- | --- | --- |
| **PIN NO.**  114, 2  67, 5, 4, 3  8  16 | **S1**  0  0  1  1 | **SYMBOL**  E  S0, S1  I0, I1, I2, I3  Y  GND  Vcc  **S0**  0  1  0  1 | **NAME & FUNCTION**  Output enable  Common data select  Data inputs  Data output  Ground (0V)  Positive supply voltage  **INPUT SELECT**  I0  I1  I2  I3 |

**Circuit Diagram:**

a) For 8-to-1-line Multiplexer using two 4-to-1 Muxes:

**Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **E** | **S1** | **S2** |  |  |  |
| **A** | **B** | **C** | **D** | **F** |  |
| 0 | 0 | 0 | 0 | 0 | **0** |
| 0 | 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 0 | 1 | **1** |
| 0 | 0 | 1 | 1 | 1 |  |
| 0 | 1 | 0 | 0 | 0 | **D** |
| 0 | 1 | 0 | 1 | 1 |  |
| 0 | 1 | 1 | 0 | 1 | **D’** |
| 0 | 1 | 1 | 1 | 0 |  |
| 1 | 0 | 0 | 0 | 1 | **1** |
| 1 | 0 | 0 | 1 | 1 |  |
| 1 | 0 | 1 | 0 | 0 | **0** |
| 1 | 0 | 1 | 1 | 0 |  |
| 1 | 1 | 0 | 0 | 1 | **D’** |
| 1 | 1 | 0 | 1 | 0 |  |
| 1 | 1 | 1 | 0 | 1 | **D’** |
| 1 | 1 | 1 | 1 | 0 |  |

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b)

For Boolean function